



Recent Developments in Semiconductor Wafer Fabrication: Materials, Processes, and Innovations

Dr. Manish Jain¹,

Associate Professor, Department of Electricals and Electronics,

Associate Professor,

Email: manish.jain@meu.edu.in

Dr. Nilesh Jain²,

Associate Professor, Department of Computer Applications,

Mandsaur University, Mandsaur (M.P.)

nileshjainmca@gmail.com

Abstract—The semiconductor industry plays a critical role in modern electronics, with semiconductor wafer fabrication being a fundamental process in integrated circuit (IC) production. This review explores the key materials, fabrication processes, and recent advancements in semiconductor wafer manufacturing. The study highlights the importance of materials such as silicon, gallium arsenide, and silicon carbide, along with emerging alternatives that enhance device performance. Additionally, advanced lithography techniques, including extreme ultraviolet (EUV) and deep ultraviolet (DUV) lithography, are discussed for their impact on miniaturization and transistor density. The paper also examines challenges in wafer fabrication, such as defect detection, process optimization, and sustainability concerns. Future research directions emphasize AI-driven manufacturing, automation, and the development of eco-friendly processes to improve efficiency and reduce environmental impact. The study sheds light on the consequences of the changing semiconductor wafer production environment for the future of electronics manufacturing.

Keywords—Semiconductor wafer fabrication, integrated circuits, lithography, silicon wafers, gallium arsenide, extreme ultraviolet (EUV) lithography, deep ultraviolet (DUV) lithography, artificial intelligence, automation, sustainable manufacturing.

I. INTRODUCTION

The electronics industry is now the largest in the world, surpassing all others. An important aspect of this industry is the manufacturing of integrated circuits. One step in making semiconductors is fabricating integrated circuits on silicon wafers. Improvements in operational processes within semiconductor manufacturing systems, smaller chips, larger wafers, and higher yield have all been targets of previous price-cutting efforts [1]. Semiconductor technology is fundamental because it forms the foundation of computer hardware. Currently, it seems that improving operating processes offers the best opportunity to achieve the necessary cost savings. A substantial initial expenditure is necessary for the semiconductor fabrication process [2].

The production of semiconductors begins with silicon wafers, which go through a series of transformations before becoming actual components [3]. The semiconductor manufacturing process focuses on fabricating integration circuits on silicon wafers. After 55 years of existence, it has grown from an obscure academic discipline into a sizable industry in its own right. In contrast to Europe, where just over

200,000 people work in the semiconductor industry, the United States employs close to 250,000. More than one million jobs in the United States and Europe are indirectly supported by this industry. The US semiconductor industry was worth \$146 billion in 2012, whereas the European industry was worth \$33 billion. Semiconductors are essential to the global electronics sector, which is worth billions of dollars. The US semiconductor industry reportedly invested \$34 billion in research and development in 2013, according to the Semiconductor Sector Association. Wafer manufacturing is the process by which integrated circuits (ICs) are made from semiconductor wafers, which are thin slices of semiconductor material, usually silicon. Several steps are involved in this intricate process, including producing the wafer, processing it, and then integrating circuits into it. At last, an IC wafer is ready to be inserted into a variety of electrical devices [4].

The manufacturing process for semiconductor wafers incorporates electrical and photonic circuits, including LEDs, optical computer components, and radio-frequency (RF) amplifiers. It is easier to build components with the required electrical designs when wafers are fabricated. In order to make chips from raw wafers, the wafer manufacturing process is essential.

The traditional technique of creating semiconductor wafers included distinct procedures for different electronic parts, including conductors, transistors, resistors, and more. These procedures, which are often separated into front-end and back-end phases, each need exact control and cutting-edge technology. Wafer fabrication is an essential part of constructing contemporary electronics because of the direct correlation between its reliability and precision and the dependability and performance of electronic devices [5]. The driving force behind the ever-changing needs of contemporary electronics, where semiconductor devices are key components of almost every technological advancement.

A. Structure of the paper

The structure of this paper is as follows: Section II overview semiconductor wafer fabrication materials process. Section III discusses the importance of semiconductor wafers. Section IV reviews literature and case studies. Section V concludes with findings and future research directions.

II. SEMICONDUCTOR WAFER FABRICATION MATERIALS PROCESS

To create ICs and other semiconductor devices utilized in contemporary electronics, a comprehensive, multi-stage process known as semiconductor wafer manufacturing is necessary. The steps required to create wafers must be carried out in a certain sequence [6]. The process of making semiconductor chips consists of five separate steps: wafer preparation, wafer fabrication, wafer sorting and testing, chip assembly and packaging, and chip testing. The process of fabricating semiconductor chips consists of both front-end and back-end processes, as shown in Figure 1 [6].

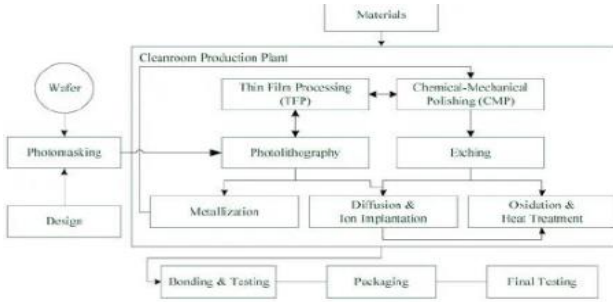


Fig. 1. Process of Semiconductor Wafer Fabrication

A scanning electron microscope (SEM) visual inspection to identify defects is therefore often performed by a professional after each of these steps in the manufacturing process. Problems with efficiency, high labor effort, lack of precision, and poor real-time performance are some of the issues with quality inspectors' manual surface inspection approaches [7].

A. Key component function of Semiconductor Wafer Fabrication

The main purposes of several of the building's components are.

- **Thin-film processing:** the technique of physically or chemically vapor-depositing crystals onto thin sheets. For CVD film thickness, several ML models were compared in. Researchers found that GPR (Lasso-Gaussian Process Regression) performed better than Boost (Gradient), Forest (Random), and Adobos. Uses tree-based models to calculate the thickness of Physical Vapour Deposition (PVD) and compares all of the results.
- **Planarization:** After deposition and etching, the surface of the wafer is smoothed using CMP. This makes sure that the surface is level and even for the next processing process. At the 45 nm, 32 nm, and 22 nm nodes, the tougher constraints on thickness, spatial homogeneity, planarity, conformance, thermal stability, and mechanical integrity must be considered throughout the planarization process.
- **Wafer Dicing and Packaging:** The wafer is cut into separate chips or dies after fabrication. After that, each die is packed for protection and external connections, allowing for incorporation into electrical equipment [8].

B. Types of semiconductor wafer

There are many different kinds of semiconductor wafers that are used in the semiconductor manufacturing process. Each form has its unique set of properties and uses [10]. The three most common types are gallium arsenide, silicon, and germanium.

- **Silicon wafers:** Solar panels, electrical components, microchips, and semiconductors are some of the many things made from silicon wafers. Furthermore, they play a role in the structural design of MEMS, which are used in the fabrication of sensors and electronics [11].
- **Germanium wafers:** Getting back to the topic at hand, germanium substrate wafers are well-suited for the production of many types of transistors, including high-frequency ones. Potential applications include infrared detectors and related optical devices [12].
- **Gallium arsenide wafers:** Additionally, it is worth noting that gallium arsenide wafers are often used in the manufacturing process of high-speed transistors and other specialized electronic devices. The production of solar cells and other gadgets that need ultra-efficient performance also makes use of them [13].

C. Fabrication Processes

The electrical measurements of the operating Nano-mechanical device prove that the two manufacturing procedures are compatible. This text is reprinted with the permission of colloidal lithography, a crucial technique for nano and micro manufacturing with huge surface areas; it allows for the self-assembly of colloids on large surfaces without the need for costly equipment [10].

- Liu et al. developed a method for optimum demanding that reduces demanding force while maintaining excellent pattern transfer fidelity and preventing deformation of soft imprinting moulds and supports. Olalla et al. suggested a method to imprint pyramidal feature composition structures with dimensions on the order of wavelengths using colloidal lithography; these structures would then be coated with a material to serve as a post-processing, post-deposition solar cell, increasing its potential usage in industrial settings [14].
- Centavo et al. suggested a scalable colloidal lithography approach for developing surfaces with efficient light trapping and hydrophobic properties that are easy, cheap cost, and operate at low temperatures [15]. Its surface characteristics' controlled nano/micro structure has significant anti-reflection and light scattering effects, which boosts average daily energy output by 35.2%.

III. THE IMPORTANCE OF SEMICONDUCTOR WAFERS

The electronic industry relies on semiconductor wafers as its fundamental substrate. Numerous items in the form of transistors, resistors, and capacitors, among other things, are created. Because of their integral role in the finished goods, these wafers determine the efficiency, dependability, and overall performance of the different electronic devices [16]. Semiconductor wafers play a crucial role in modern electronics, forming the foundation for integrated circuits (ICs) and microchips. These thin, disc-shaped substrates are

made primarily from silicon, though other materials such as GaAs and SiC are also used for specialized applications.

A. Materials of semiconductor wafers

Highly refined single crystals are used to make semiconductor wafers. A wide range of materials are used, the most prevalent of which is silicon.

- **Germanium:** Optoelectronics and high-speed electronics both need high carrier mobility.
- **Gallium Arsenide (GaAs):** Frequently used in RF and microwave devices because to its efficiency at high frequencies and temperatures [17].
- **Silicon Carbide (SiC):** Power electronics benefit greatly from its high breakdown voltage and exceptional heat conductivity.
- **Indium Phosphide (InP):** Extremely mobile electrons, used in high-frequency, high-speed systems like fiber optics
- **Silicon Germanium (SiGe):** Powers up transistors, which are a staple of high-speed integrated circuits [18].
- **Sapphire (Al₂O₃):** A substrate used in the production of optoelectronics and LEDs due to its excellent thermal stability and insulating qualities.
- **Gallium Nitride (GaN):** Excellent power management and efficiency, necessary for light-emitting diodes and power transistors.
- **Zinc Oxide (ZnO):** Optoelectronic uses for this transparent semiconductor include transparent thin-film transistors and ultraviolet detectors [19].
- **Diamond:** Highly mobile electrons and very good thermal conductivity; used in high-frequency, high-power devices. The development of several semiconductor technologies that are essential to contemporary electronics is made possible by these materials [10].

B. Wafer Fabrication Techniques used in semiconductor

There are hundreds of phases in the manufacturing process of semiconductor wafers, and each one involves a complex technique. These operations include oxidation, photolithography, cleaning, etching, and planarization, among many others. When making semiconductor wafers, each one goes through a series of mechanical operations called "process steps," which are also called "unit processes." [20]. There are usually more than 500 manufacturing steps involved in the creation of semiconductor wafers. The manufacture of semiconductor wafers is an intricate process that transforms silicon, gallium arsenide, and germanium into miniature devices. Constructing photonic or electrical circuits on semiconductor wafers is a lengthy process [21]. New developments in wafer fabrication technology are detailed here:

1) Lithography Innovations

There would be no semiconductor industry without lithography, an essential enabling technology. There is no way to make ULSI circuits without the lithography step of semiconductor wafer fabrication. Immediate results include smaller features and higher transistor densities. Additional applications of optical lithography are being explored via the use of 157 nm technology for nodes ranging from 65 nm to 45 nm [22].

2) Deep Ultraviolet (DUV) and Extreme Ultraviolet (EUV) lithography

DUV and EUV lithography are advanced photolithography techniques used in semiconductor manufacturing to create extremely small and precise circuit patterns on wafers. DUV lithography operates at wavelengths such as 193 nm (ArF laser) and is widely used for fabricating chips at nodes up to 7 nm with multiple patterning techniques. EUV lithography, on the other hand, uses a much shorter wavelength of 13.5 nm, enabling direct patterning of smaller features down to 2 nm, reducing the need for complex multiple patterning. EUV allows higher transistor density, improved power efficiency, and performance in modern chips, making it essential for next-generation semiconductor manufacturing [23].

IV. LITERATURE REVIEW

This section provides the previous research on Developments in Semiconductor Wafer Fabrication. This Table I provides a structured comparison of the reviewed literature, outlining their key focus areas, contributions, and avenues for future research.

In this study, Pan et al. (2018) analyze cluster tools' scheduling and modeling approaches, including both revisiting and non-revisiting approaches. After that, their approaches to solving the problem are examined and contrasted. Prior to delving into revisiting procedures, this article addresses the scheduling issue of certain generic production systems that include revisiting. Finally, the conclusion and future directions of the study are addressed. As a word to the wise, semiconductor production systems are among the most intricate and cutting-edge in the industry. They rely on cluster tools that are powered by highly automated robots. It is hard to plan and manage them due to factors such as wafer residence time limits, wafer revisiting, activity time volatility, chamber cleaning needs, and PMs that are prone to failure[24].

In this study, Taha, (2018) suggests a method for evaluating the semiconductor manufacturing process known as CDID. In a particular manufacturing processing step, an inline inspection tool may detect a cluster of defects; CDID can determine which carry-over defect class was responsible for these clusters. The first step for CDID is to determine the kind of Rx defect by comparing the Rx picture with reference wafer maps of previously acquired defect clusters. Applying the laws of inference triggers the premises. To find the source of d, CDID uses the inference rules to apply the defect definition rules recursively[25].

In this study, Wang (2023) combination of two-dimensional materials, especially graphene, with silicon CMOS circuits might radically alter the history of electronic devices. This presentation delves into the use of Back-End-of-Line (BEOL) processing to include these materials seamlessly, showcasing their compatibility and performance advantages. The importance of this development is highlighted by the expected economic changes in the markets for graphene-based applications that include silicon. They are moving closer to a future where 2D materials expand the boundaries of technology as recent advances tackle critical issues in wafer-scale production[26].

In this study, Noori et al. (2024) examine the processes involved in the creation of semiconductor technologies, which

may include hundreds or even thousands of steps carried out by pipelines that may make use of hundreds of fabrication tools. Size and price of semiconductor wafers may vary greatly according to their components and intended use. The installation and running expenses of a facility's fabrication machines that can process wafers of any size and material might be somewhat significant. This study presents a technique for processing arbitrary-sized and material wafers in fabrication facilities meant for big wafers with little tool contamination[27].

In this study, Maslov, Yugma and Vialletelle (2023) detail a novel method for aligning data during wafer creation, the first step of semiconductor production. Semantic modeling forms the basis of this method, which focuses on formalizing technical information by means of an ontology network for the

purpose of describing wafer fabrication equipment. This paper presents a technique for building such a model and uses a real-world application for STMicroelectronics to demonstrate how to check that the model is consistent[28].

In this study, Bardhan et al. (2021) examine a scheduling and production planning issue in a semiconductor wafer manufacturing facility that processes several products. The facility handles difficult aspects such as various re-entrant loops and equipment characteristics. Iterative execution of the planning and simulation stages closes the performance gap between the projected production level and the simulation output. The current status of work-in-process (WIP) or production is used to determine a wafer's priority according to a suggested scheduling rule[29].

TABLE I. LITERATUREITERATURE ON DEVELOPMENTS IN SEMICONDUCTOR WAFER FABRICATION

References	Focus Area	Key Contribution	Limitations & Future Work
[24]	Scheduling for cluster tools of semiconductor wafer	Review scheduling methods for no-revisiting and revisiting wafer processes	Need for advanced automation and optimization techniques to handle complex scheduling constraints
[25]	Defect diagnosis in semiconductor fabrication	Introduces CDID system for identifying defect sources using in-line inspection tools	Requires further refinement to enhance defect identification accuracy using AI-based improvements
[26]	2D materials integration with CMOS in wafer fabrication	Discusses graphene-silicon integration via BEOL processing	Challenges in large-scale fabrication and ensuring seamless integration for commercial applications
[27]	Processing wafers of varying sizes and materials	Develops a method for processing wafers of various dimensions while minimizing contamination	Further research needed for scalability and contamination control across different materials
[28]	Data alignment in wafer fabrication	Introduces a semantic modeling approach using ontologies	Improvements needed in interoperability and standardization of ontology-based modeling
[29]	Production planning and scheduling in semiconductor	Presents an iterative scheduling method based on work-in-process (WIP) state	Potential for AI-driven scheduling models to enhance production efficiency

V. CONCLUSION AND FUTURE WORK

The continuous evolution of semiconductor wafer fabrication is crucial for sustaining the rapid advancements in electronics and computing technology the semiconductor industry has evolved significantly over the past decades, with semiconductor wafer fabrication being a fundamental process in modern electronics manufacturing. The role of semiconductor wafers in the production of integrated circuits and other electronic components cannot be overstated, as they directly impact the efficiency, reliability, and performance of various technological applications. The advancements in wafer fabrication technologies, including lithography innovations and DUV and EUV lithography, have contributed to the continuous miniaturization and enhancement of semiconductor devices. The various fabrication techniques, including thin-film processing, planarization, and wafer dicing, play an essential role in ensuring the precision and quality of semiconductor wafers. Improved defect identification, quality assurance, and process optimization have also resulted from an integration of AI and ML methods in semiconductor production. While semiconductor manufacturing has made remarkable progress, challenges such as high production costs, stringent quality requirements, and increasing demand for smaller and more efficient devices remain. Addressing these challenges will require continued research and technological innovation to further enhance semiconductor fabrication processes.

Future research in semiconductor wafer fabrication should focus on advancing sustainable and cost-effective manufacturing techniques while enhancing process efficiency and precision. Integration of AI and ML into fabrication processes can optimize defect detection, predictive

maintenance, and yield enhancement. Additionally, research should explore novel materials beyond traditional silicon, such as gallium nitride (GaN) and two-dimensional materials like graphene, to improve semiconductor performance and energy efficiency.

REFERENCES

- [1] Muthuvel Raj Suyambu and Pawan Kumar Vishwakarma, "Improving Efficiency of Electric Vehicles: An Energy Management Approach Utilizing Fuzzy Logic," *Int. J. Adv. Res. Sci. Commun. Technol.*, vol. 3, no. 2, pp. 737–748, Feb. 2023, doi: 10.48175/IJARSCT-9749V.
- [2] H. J. Yoon and J. Chae, "Simulation study for semiconductor manufacturing system: Dispatching policies for a wafer test facility," *Sustain.*, 2019, doi: 10.3390/su11041119.
- [3] D. H. Shih, C. Y. Yang, T. W. Wu, and M. H. Shih, "Investigating a Machine Learning Approach to Predicting White Pixel Defects in Wafers—A Case Study of Wafer Fabrication Plant F," *Sensors*, vol. 24, no. 10, 2024, doi: 10.3390/s24103144.
- [4] J. W. Fowler, L. Mönch, and T. Ponsignon, "Discrete-event simulation for semiconductor wafer fabrication facilities: A tutorial," *Int. J. Ind. Eng. Theory Appl. Pract.*, vol. 22, no. 5, pp. 661–682, 2015.
- [5] T. Chen, "Strengthening the competitiveness and sustainability of a semiconductor manufacturer with cloud manufacturing," *Sustain.*, 2014, doi: 10.3390/su6010251.
- [6] S. Lee and D. H. Lee, "Path Score Based Approach for Deriving Machine Sequence in Multistage Process," *Lect. Notes Bus. Inf. Process.*, vol. 507 LNBIP, pp. 60–70, 2024, doi: 10.1007/978-3-031-58113-7_6.
- [7] F. López de la Rosa, R. Sánchez-Reolid, J. L. Gómez-Sirvent, R. Morales, and A. Fernández-Caballero, "A review on machine and deep learning for semiconductor defect classification in scanning electron microscope images," *Appl. Sci.*, vol. 11, no. 20, pp. 1–21, 2021, doi: 10.3390/app11209508.
- [8] V. Panchal, "Energy-Efficient Core Design for Mobile

- Processors : Balancing Power and Performance,” pp. 191–201, 2024.
- [9] A. Emami-Naeini and D. De Roover, “Control in Semiconductor Wafer Manufacturing,” *Comput. Sci. Eng.*, 2008, [Online]. Available: https://www3.nd.edu/~pantsakl/Archive/WolovichSymposium/files/Emami_Paper.pdf
- [10] H. S. Chandu, “A Survey of Semiconductor Wafer Fabrication Technologies : Advances and Future Trends,” *IJRAR*, vol. 10, no. 4, pp. 344–349, 2023.
- [11] Y. Jingfei, B. Qian, L. Yinnan, and Z. Bi, “Formation of subsurface cracks in silicon wafers by grinding,” *Nanotechnol. Precis. Eng.*, 2018, doi: 10.1016/j.npe.2018.09.003.
- [12] C. Sanchez-Perez, I. Garcia, and I. Rey-Stolle, “Fast chemical thinning of germanium wafers for optoelectronic applications,” *Appl. Surf. Sci.*, 2022, doi: 10.1016/j.apsusc.2021.152199.
- [13] C. Guo *et al.*, “Photoelectric effect accelerated electrochemical corrosion and nanoimprint processes on gallium arsenide wafers,” *Chem. Sci.*, 2019, doi: 10.1039/c9sc01978b.
- [14] H. Sarpana Chandu, “Robust Control of Electrical Machines in Renewable Energy Systems: Challenges and Solutions,” *Int. J. Innov. Sci. Res. Technol.*, vol. 09, no. 10, pp. 594–602, Oct. 2024, doi: 10.38124/ijisrt/IJISRT24OCT654.
- [15] Y. Ma *et al.*, “A Review of Advances in Fabrication Methods and Assistive Technologies of Micro-Structured Surfaces,” 2023. doi: 10.3390/pr11051337.
- [16] M. Z. Hasan, R. Fink, M. R. Suyambu, M. K. Baskaran, D. James, and J. Gamboa, “Performance evaluation of energy efficient intelligent elevator controllers,” in *IEEE International Conference on Electro Information Technology*, 2015. doi: 10.1109/EIT.2015.7293320.
- [17] C. W. Cheng, K. T. Shiu, N. Li, S. J. Han, L. Shi, and D. K. Sadana, “Epitaxial lift-off process for gallium arsenide substrate reuse and flexible electronics,” *Nat. Commun.*, 2013, doi: 10.1038/ncomms2583.
- [18] H. S. Chandu, “A Review on CNC Machine Tool Materials and Their Impact on Machining Performance,” *Int. J. Curr. Eng. Technol.*, vol. 14, no. 5, pp. 313–319, 2024.
- [19] R. Dattangire, R. Vaidya, D. Biradar, and A. Joon, “Exploring the Tangible Impact of Artificial Intelligence and Machine Learning: Bridging the Gap between Hype and Reality,” *2024 1st Int. Conf. Adv. Comput. Emerg. Technol. ACET 2024*, pp. 2024–2025, 2024, doi: 10.1109/ACET61898.2024.10730334.
- [20] Muthuvel Raj Suyambu and Pawan Kumar Vishwakarma, “Improving grid reliability with grid-scale Battery Energy Storage Systems (BESS),” *Int. J. Sci. Res. Arch.*, vol. 13, no. 1, pp. 776–789, Sep. 2024, doi: 10.30574/ijra.2024.13.1.1694.
- [21] J. Kim and I. Joe, “Chip-Level Defect Analysis with Virtual Bad Wafers Based on Huge Big Data Handling for Semiconductor Production,” *Electron.*, vol. 13, no. 11, 2024, doi: 10.3390/electronics13112205.
- [22] V. Panchal, “Mobile SoC Power Optimization : Redefining Performance with Machine Learning Techniques,” vol. 13, no. 12, 2024, doi: 10.15680/IJIRSET.2024.1312117.
- [23] G. Dattoli *et al.*, “Extreme ultraviolet (EUV) sources for lithography based on synchrotron radiation,” *Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip.*, 2001, doi: 10.1016/S0168-9002(01)00887-7.
- [24] C. R. Pan, M. C. Zhou, Y. Qiao, and N. Q. Wu, “Scheduling Cluster Tools in Semiconductor Manufacturing: Recent Advances and Challenges,” *IEEE Trans. Autom. Sci. Eng.*, 2018, doi: 10.1109/TASE.2016.2642997.
- [25] K. Taha, “CdId: A system for identifying the root cause of a defect in semiconductor wafer fabrication,” *IEEE Trans. Semicond. Manuf.*, 2018, doi: 10.1109/TSM.2018.2808703.
- [26] Z. Wang, “Wafer-Scale Integration of 2D Materials for Application in High-Performance Electronics and Optoelectronics,” in *2023 IEEE Nanotechnology Materials and Devices Conference, NMDC 2023*, 2023. doi: 10.1109/NMDC57951.2023.10343789.
- [27] Y. J. Noori, I. Skandalos, X. Yan, N. Zhelev, Y. Hou, and F. Gardes, “Wafer Bonding for Processing Small Wafers in Large Wafer Facilities,” *IEEE Trans. Components, Packag. Manuf. Technol.*, 2024, doi: 10.1109/TCPMT.2023.3341329.
- [28] G. Maslov, C. Yugma, and P. Vialletelle, “Semantic modeling for smart manufacturing: Towards a data alignment through knowledge formalization for semiconductor wafer fabrication,” in *ASMC (Advanced Semiconductor Manufacturing Conference) Proceedings*, 2023. doi: 10.1109/ASMC57536.2023.10121118.
- [29] R. Bardhan, C. Xu, Z. Cao, and P. S. Tan, “An Iterative Scheme for Hierarchical Production Planning in Semiconductor Wafer Fabrication,” in *2021 IEEE International Conference on Industrial Engineering and Engineering Management, IEEM 2021*, 2021. doi: 10.1109/IEEM50564.2021.9672987.