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RESEARCH PAPER

High-Accuracy based on Deep Learning Techniques for Pattern Recognition of Wafer Defect

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***Abstract*—In semiconductor production, automated wafer defect pattern detection is a crucial procedure that improves product quality, yield, and efficiency. The paper introduces a powerful deep learning-powered system of classifying wafer defects based on a 1D-Convolutional Neural Network (1D-CNN). The WM-811K wafer map dataset, the biggest publicly available dataset based on actual wafer manufacturing processes in industry, is used to assess the suggested approach. Data analysis and visualization are first conducted comprehensively regarding the distribution of wafer index, frequencies of defects and patterns of spatial failures. A large preprocessing pipeline is used to guarantee the reliability and consistency of data, such as data cleaning, filtering out non-defective and inaccurate samples of failure types, remapping pixel values to grayscale, converting the grayscale to RGB, image resizing and data augmentation. These procedures are highly successful in raising dataset quality and model generalization. The 1D-CNN model is trained to efficiently acquire discriminative defect features after the filtered data is divided into training and testing data. The following measures are used to evaluate the model's performance: accuracy, precision, recall, F1-score, loss, and AUC-ROC. Results of the experiment indicate that the suggested 1D-CNN has 99.0% accuracy and 99.0% AUC-ROC, which is superior to several other cutting-edge methods. The results indicate the practical applicability, soundness, and efficacy of the suggested framework in automated inspection of defects in the wafer of semiconductor manufacturing.**

Keywords—Wafer Defect Pattern Recognition, Semiconductor Manufacturing, Deep Learning, Wafer Map Analysis, Automated Inspection, Defect Classification.

I. INTRODUCTION

Wafers are regarded as a significant resource in the semiconductor industry as they are the most important semiconductor material. The two types of wafers are prime wafers and test wafers [1]. The test wafers are further divided into two categories: control (monitor) and counterfeit wafers. Although integrated circuits are built using prime wafers, test wafers are mostly used to maintain machinery and verify parameters throughout the production process. However, only test wafers can be recovered because the prime wafer was converted into IC chips [2]. Increased reusability boosts the IC foundries' profits and, consequently, their competence. Recycling or reclaiming wafers is important since they are a precious and finite resource that may drastically reduce production costs [3]. In other words, Increased reusability boosts the IC foundries' profits and, consequently, their competence.

Expert inspectors frequently carry out the manual early detection of wafer surface flaws, which have drawbacks including high cost, high subjectivity, low efficiency, and poor precision that cannot meet the standards of modern industrialized goods. Currently, machine vision-based defect detection methods replace manual inspection in the field of wafer inspection. In semiconductor production, wafer surface defect detection is crucial to maintaining product quality and has emerged as a key area of computer vision research [4]. Conventional machine vision-based fault detection techniques frequently rely on labor-intensive human feature extraction.

Silicon wafers, which go through several steps to become semiconductor components, are essential to the production of semiconductors. The dynamics of the semiconductor industry are linked to the expansion of the industry. Recent constraints in the semiconductor chain have affected advanced and mature wafer manufacturing capacity due to Increased safety stockpiles and cautious supply-side expansion due to COVID-19. The quality of wafers, the basic building block of semiconductors, is decided after many stages of manufacturing and is impacted by a number of variables, such as staff, equipment, and timetable. Significant losses result from defects that frequently go undetected until after wafers are utilized by consumers [5]. The tolerance for metal contamination declines with the complexity and size of semiconductor components, potentially resulting in issues with quality.

Preventive maintenance, reducing downtime, and lowering maintenance costs all depend on artificial intelligence [6] monitoring and prediction capabilities [7]. Corporate production efficiency and competitiveness are enhanced by technology that blends AI and AOI [8] in the highly competitive global market. The method is also applicable to other high-precision production fields, including aerospace manufacturing, biomedicine, and sophisticated semiconductors [9][10][11]. This technology offers more technical innovation. In recent years, DL inspection methods[12] are embodied in CNN, which have become the industry standard for identifying defects in semiconductor production processes because to their high-speed automation, low cost, high accuracy, and non-contact nature [13].

A. Motivation and Contribution of the Paper

Wafers are a rare and valuable material in the production of semiconductor devices, and thus early and correct fault detection is necessary to enhance the yield, minimize the price, and facilitate the successful reuse of the wafers. Manual inspection is inefficient, subjective, and expensive; and the conventional machine vision approaches based on manually-

designed features are not very robust to complex-shaped defects. As the complexity of wafer and quality requirements increases, defects can go unnoticed until late and lead to huge losses. These issues inspire this study, as it aims at creating an effective deep learning-based solution to automated wafer defect pattern recognition in to improve inspection's precision, dependability, and industry applicability. The main contributions are:

- Analysis and collection of a large-scale WM-811K dataset of wafer map (large scale) the largest publicly accessible dataset of wafer production processes.
- Design of a powerful data preprocessing pipeline, such as data cleaning, mapping pixel values, converting to RGB, resizing of images, and data augmentation to increase the model's resilience and the caliber of the data.
- Design and implementation of an efficient 1D-CNN–based classification framework for automated wafer defect pattern recognition.
- Large-scale performance evaluation based on a number of parameters, including learning curves, confusion matrix analysis, recall, accuracy, precision, F1-score, loss, and AUC-ROC.

B. Significance of the Study

The proposed research is important because it introduces a well-operating and trustworthy deep learning framework to recognize the pattern of automated wafer defects on a large scale of a realistic dataset. The proposed methodology shows good generalization and is characterized by high classification accuracy due to the use of rigorous data preprocessing, meaningful visualization, and a well-designed 1D-CNN model. The findings reveal the evident betterment of the current approaches, which illustrates the strength of the model and its feasibility. Overall, the work is a contribution to the development of intelligent wafer inspection systems and faster and more accurate defect detection that can potentially improve yield and reduce the cost of inspection as well as quality assurance in the manufacturing of semiconductors.

C. Structure of the Paper

The paper is structured as follows: Section II presents the related literature in the field of Wafer Defect Pattern Recognition. Section III describes the methods, supplies and processes. Section IV provides discussion, outcomes and analysis of the proposed system along with the experimental data. Section V outlines the last considerations and intentions.

II. LITERATURE REVIEW

In this section, Table I summarizes the literature review of recent works in Wafer Defect Pattern Recognition. It summarizes the problem, methodology, dataset, and the main findings, which were discussed in the reviewed works.

Lee et al. (2025) initially introduced a novel feature extraction strategy that leverages features extracted by the CNN model, Density-based features, and Radon-based features, effectively capturing structural and spatial characteristics in wafer defect patterns. Second, propose an ensemble learning framework integrating multiple classifiers with optimized weighting mechanisms to enhance classification robustness. Third, provide empirical evidence demonstrating that the weighted soft voting approach achieves superior performance, attaining a classification accuracy of 95.09% and an F1 score of 0.95%. These findings confirm the approach's efficacy in raising wafer defect classification reliability, which is essential for developing automated defect inspection in semiconductor production [14].

Ni et al. (2025) proposed a technique for augmenting data to increase the effectiveness of overlapping fault detection. This method effectively addresses the difficulty of identifying multipattern flaws in the semiconductor industry. Experimental findings, utilizing the universal defect dataset MixedWM38, demonstrate that the recommended method achieves an accuracy of 89.3% for overlapped type recognition, coupled with an impressive 89% mean average precision (mAP) for defect localization [15].

Kumar et al. (2024) suggested an innovative technique for semiconductor wafer surface defect assessment using deep convolutional neural networks. It is necessary to first construct a special structure for feature pyramid networks with atrous convolution (FPNAC) in order to extract features and produce feature maps. In order to generate region ideas, the feature plots must be sent into the region proposal network (RPN) in the second stage. The region suggestions are then linked to matching size utilizing the inputs of a three-branch Radial Basis Functional Neural Network (RBFNN) in order to accurately classify and separate the defects. The testing results show that the proposed RBFNN performs well overall, with Mean Pixel Accuracy (MPA) of 94.97% and Mean Intersection over Union (MIoU) of 90.06% [16].

Dubey et al. (2024) demonstrated initial work on wafer defect detection. The dataset is captured using an infrared (IR) camera, which makes it quick to analyze the bond interface for any abnormality. A ResNet-based artificial intelligence model for panoptic segmentation is then adapted by training on this data for defect identification and classification. ResNet-based model can identify and make a distribution plot of the defects based on the class defined with up to 95% accuracy for large-size defects [17].

Batool et al. (2023) proposed a model that improves the discriminative feature learning of complex errors using attention-augmented convolutional neural networks (A2CNN). The A2CNN model emphasizes the channel and spatial dimensions. Additionally, the model employs a customized loss function to reduce misclassification and a global average pooling layer to enhance the network's generalization by avoiding overfitting. The A2CNN model is evaluated on the MixedWM38 wafer defect dataset using 10-fold cross-validation. It performs exceptionally well, with accuracy, precision, recall, and F1-score values of 98.66%, 99.0%, 98.55%, and 98.82%, respectively. The A2CNN model outperforms previous research by efficiently learning useful information for intricate mixed-type wafer faults [18].

Li et al. (2022) suggested the importance of root cause analysis in yield learning, may be performed using wafer failure pattern recognition. Test DNA was recently suggested as a way to enhance diagnostic resolution using wafer test data. Prior research on machine learning-based wafer failure pattern detection has shown good classification outcomes. In this letter, suggest using ensemble learning techniques and geographical information to improve classification accuracy. According to experimental findings, the suggested approach can increase accuracy by 8.9%[19].

A. Research Gaps

Current literature usually utilizes complicated architectures or feature engineering on a large scale, making them difficult to scale or deploy in real-time. Most of the approaches do not have strong pre-processing and are unable to generalize patterns of defects. This necessitates the need to find a simpler, computationally efficient, and highly accurate framework that makes sure of a reliable classification of wafer defects to be depended on by the industry.

TABLE I. EXISTING LITERATURE STUDIES ON WAFER DEFECT PATTERN RECOGNITION

Authors & Year	Proposed Method	Dataset	Key Contributions	Performance
Lee et al. (2025)	CNN feature extraction combined with density-based and Radon-based features; weighted soft voting ensemble	Wafer defect dataset	Integrated structural and spatial features with ensemble learning to improve robustness	Accuracy: 95.09%, F1-score: 0.95
Ni et al. (2025)	Data augmentation for overlapped defect recognition	MixedWM38	Improved recognition of multi-pattern and overlapped defects	Accuracy: 89.3%, mAP: 89%
Kumar et al. (2024)	FPN with atrous convolution (FPNAC) + RPN + RBFNN	Semiconductor wafer images	Joint detection, segmentation, and classification of defects	MIoU: 90.06%, MPA: 94.97%
Dubey et al. (2024)	ResNet-based panoptic segmentation using IR imaging	IR wafer defect dataset	Fast defect detection and classification using infrared imaging	Accuracy: up to 95% (large defects)
Batool et al. (2023)	Attention-Augmented CNN (A2CNN) with focal loss	MixedWM38	Enhanced channel and spatial feature learning for complex defects	Accuracy: 98.66%, F1: 98.82%
Li et al. (2022)	Spatial feature learning with ensemble algorithms	Wafer test data	Improved failure pattern recognition for root cause analysis	Accuracy improvement: +8.9%

III. METHODOLOGY

The proposed methodology start by retrieving the WM-811K wafer map data in Kaggle and first visualizing the information to understand fault trends. Subsequently, the data is processed by preprocessing, which involves cleaning and filtering of data, mapping of pixel values, converting the data to a different format and resizing the images. The model's generalization is enhanced by data augmentation once the processed data is separated into training (80%) and testing (20%) sets. Evaluation of the model's accuracy, precision, recall, f1-score performance, and loss following the training of a 1D CNN model using the processed data yields the final findings. The suggested methodology's flowchart is displayed in Figure 1.

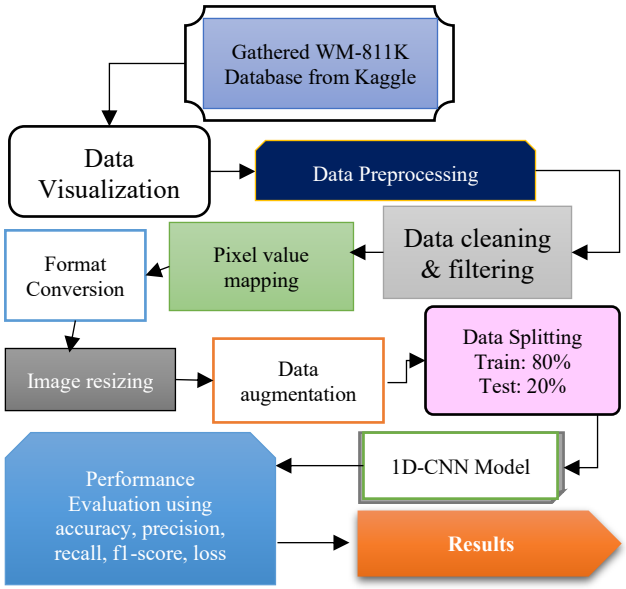


Fig. 1. Flowchart of Wafer Defect Pattern Recognition

This section explains the following phases of the flowchart in a nutshell:

A. Data Analysis and Visualization

This study uses the WM-811K wafer dataset, which is the biggest wafer map dataset presently available to the public, for both testing and training. The dataset, which includes 811,457 samples with 9 defect types, is taken from the actual wafer fabrication process; only around 21% of the samples have labels. The data visualizations are shown below:

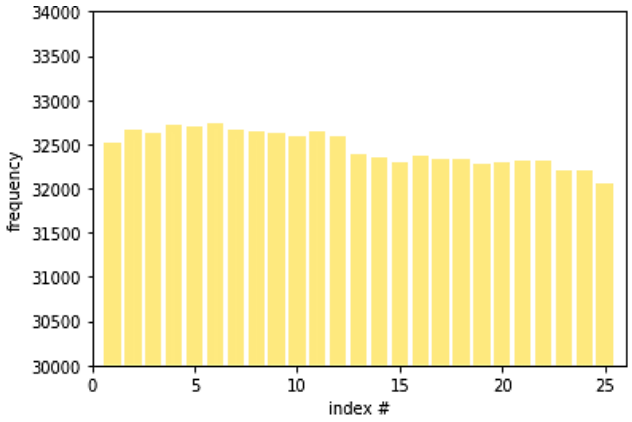


Fig. 2. Wafer Index Distribution

The frequency distribution of the various index values is shown in Figure 2. The bar chart reflects fairly regular frequencies with slight variations, which are indicative of an equal distribution among indices. There is also a minor downward trend towards more index values, indicating minor fluctuation as opposed to a major imbalance. Overall, the number is representative of a well-distributed and steady dataset that can be analyzed.

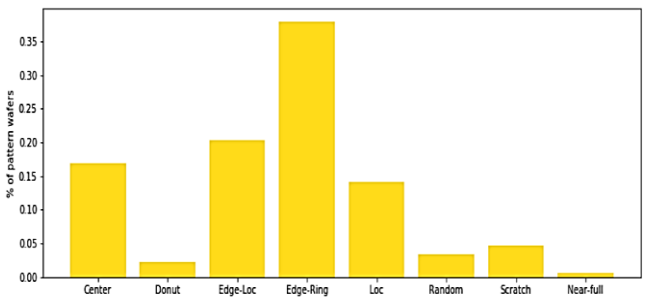


Fig. 3. Failure Type Frequency

According to Figure 3, Edge-Ring is the most prevalent pattern, and it is followed by Edge-Loc and Centre, whereas Loc is moderately represented. The other patterns are quite rare with Near-full being close to extinction.

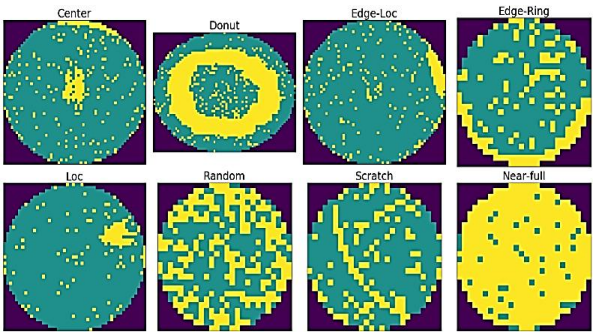


Fig. 4. Wafer Failure Type Pattern

Figure 4 is an example of the spatial distribution of the various types of shapes emphasizing the various distinct shapes of defect, such as central clustering, rings, edge-localized, edge-ring, localized pots, random scattering, linear scratch-like shapes and near-uniform coverage over the surface.

B. Data Preparation

Data processing is necessary to prepare the dataset for modelling and analysis in order to guarantee reliable and accurate results, particularly when handling differences in wafer map dimensions and defect pattern frequencies.

- **Data cleaning and filtering:** Data has been cleaned and filtered to be left with only actual defect patterns by eliminating wafer maps, which had no defects, or had incorrect defect patterns (types of failure). This left 25,519 valid images of wafer maps.
- **Pixel value mapping:** A mapping of original grayscale wafer maps to three discrete intensity levels (0, 127, and 255), which display black, mid-gray, and white, was done to improve contrast and visualization. Equation (1) explains it:

$$pixel\ value = \begin{cases} 0 \rightarrow & 0 \\ 1 \rightarrow & 127 \\ 2 \rightarrow & 255 \end{cases} \quad (1)$$

- **Format conversion:** The grayscale images were transformed to RGB format such that they could be used in the DL models.
- **Image resizing:** Image size is different between wafer maps; therefore, all images were re-sampled to 56 × 56 with bicubic.
- **Data augmentation:** Geometric and intensity-based transformations were used to create new training examples and enhance model generalization and reduce overfitting.

C. Data Splitting

To ensure an equitable representation of the various fault categories, the dataset was divided into training and testing sets, 80:20.

D. Proposed Classification Framework: 1D-CNN

To handle the 1-dimensional data, 1D-CNN is composed of activation functions, dropout layers, pooling layers, and 1-dimensional convolution layers. The hyperparameters for 1D-CNN are as follows: size of the filter, number of CNN layers, neurons in each layer, and subsampling factor of each layer [20]. The convolution layer is the basic mechanism by which a filter is applied to an input. Applying the filtering procedure repeatedly results in a feature map that highlights the particular attributes connected to the data points. Convolution is a linear process that uses a set of weights to limit the multiplication of inputs. In this instance, inputs are multiplied by the kernel, which is a single-dimensional array of weights. A feature map is produced by carrying out this procedure, which provides a distinct value for every pass. The ReLU activation function receives each value after the feature map has been computed. ReLU is a linear activation function that returns the same input if it is not negative, otherwise converting it to zero. The ReLU activation function solves the vanishing gradient issue, improves model performance, and speeds up learning from the training data. It is demonstrated using Equation (2) as follows:

$$R(z) = \max(0, z) \quad (2)$$

Here, z is the input being received by the activation function, and $R(z)$ is the activation function's positive output.

IV. Performance Evaluation and Result Analysis

The experiment uses an AMD Ryzen 7 3700X 8-Core CPU with 16GB RAM running at 3.59 GHz and an NVIDIA GeForce RTX 2070 SUPER GPU running Windows 10. In a Python 3.10.9 environment, the DL frameworks utilized are TensorFlow 2.15.0 and Keras 2.15.0.

A. Performance Evaluation

There is continuous improvement in 1D-CNN models' classification performance for wafer map defect detection. This entails enhancing ROC analysis, f1-score, recall, accuracy, and precision. A confusion matrix depicts a concise evaluation of a deep learning model's performance using a specific dataset for testing purposes. It is extensively utilized to evaluate the effectiveness of classification models. For each input event, these models provide predictions of categorical labels.

- **Accuracy:** Accuracy describes how well a model can classify every occurrence in a dataset. To calculate it, divide the total number of projections by the number of forecasts that are accurate. The accuracy is determined using Equation (3):

$$Accuracy = \frac{TP+TN}{TP+FP+TN+TN} \quad (3)$$

- **Precision:** Precision is a measure of the proportion of the items that are or are expected to be positive. The mathematical formula in Equation (4) is presented in the following:

$$Precision = \frac{TP}{TP+FP} \quad (4)$$

- **Recall:** The number of right answers that were truly positive is known as recall. The formula is given in Equation (5):

$$Recall = \frac{TP}{TP+FN} \quad (5)$$

- **F1-Score:** The accuracy and recall harmonic means are taken to determine the F1 score. While accuracy quantifies recall counts, the number of real positive events that are accurately classified as positive, it is the proportion of correctly anticipated positive occurrences among all projected positive instances. The F1 score is calculated using in Equation (6):

$$F1 - Score = 2 * \frac{Precision*Recall}{Precision+Recall} \quad (6)$$

- **Loss:** The loss function calculates the discrepancy between the actual labels and the model's anticipated outputs, guiding the optimization process by minimizing prediction errors during training.

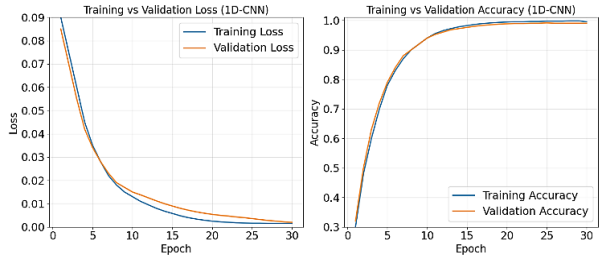
where FP is TP is the number of correctly predicted positive instances, TN is the number of correctly predicted negative instances, FN is the number of positive cases that are mistakenly classified as negative, and the number of negative cases that are mistakenly classified as positive.

B. Results Analysis

Table II shows the result of the 1D-CNN model for wafer defect pattern recognition. The model achieved 99.0% accuracy and 99.0% AUC-ROC, indicating a high level of discriminative capacity. All three measures, precision, recall, and F1-score, were 97.0% and therefore showed balanced and credible defect classification. In general, the findings support the usefulness of the 1D-CNN method in automated inspection of wafer defects.

TABLE II. MODEL PERFORMANCE ON WAFER DEFECT PATTERN RECOGNITION

Metrics	1D-CNN
Accuracy	99.0
Precision	97.0
Recall	97.0
F1-Score	97.0
AUC-ROC	99.0



(a)Loss (a)Accuracy

Fig. 5. (a) Loss and (b) Accuracy Curves of the 1D-CNN

The 1D-CNN model's accuracy curves over epochs are shown in Figure 5. The loss plot demonstrates effective learning and steady optimization with a steep decline in training and validation loss during the early epochs, followed by a smooth convergence to minimum values. Correspondingly, the accuracy plot shows a sharp rise in performance, with training and validation accuracies approaching 99%. The close alignment between training and validation curves in both plots highlights good generalization and the absence of overfitting.

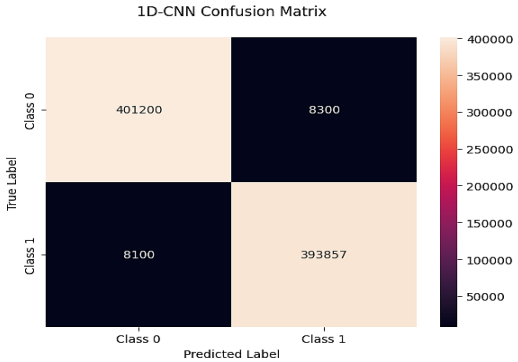


Fig. 6. Confusion Matrix of the 1D-CNN

The proposed 1D-CNN model is characterized by a strong ability to classify, as indicated in Figure 6 below. The model has a high number of correct predictions with 401,200 true negatives and 393,857 true positives, and misclassifications are low. The prevailing diagonal structure attests to the soundness of the model and the good discrimination ability of Class 0 and Class 1.

C. Comparative Analysis and Discussion

Table III compares the performance of the different models that are used to recognize wafer defect patterns. The previous methods, like Feature Fusion CNN and LeNet, have moderate characteristics of 84.98 and 85.7 percent classification, respectively, whereas the more recent MFFP-Net has a much higher percentage of 96.71. It is also competitive with other compared models because the proposed 1D-CNN model has the highest accuracy of 99.0 of recognition wafer defect patterns.

TABLE III. COMPARISON OF MODELS IN WAFER DEFECT PATTERN RECOGNITION

Model	Accuracy
Feature Fusion CNN (2-layer, filter 16) [14]	84.98
LeNet [21]	85.7
MFFP-Net [22]	96.71
1D-CNN	99.0

D. Discussion

The experimental results confirm that the suggested 1D-CNN model works well for spotting wafer defect patterns. The model has high discriminative capability and balanced classification, quick and consistent convergence, and excellent generalization with no overfitting. The confusion table also confirms that there is a strong separation in classes with few misclassifications. Taken together, the suggested strategy is better than the current mechanisms, which highlights its appropriateness in terms of credible and workable automated wafer inspection.

V. CONCLUSION AND FUTURE DIRECTION

The map of defects on a wafer defines the distribution, kind, and wafer surface defect position, which form the basis of the defect detection state as they enable a methodical examination of the defect patterns. This paper has managed to achieve a successful deep learning-based solution to automatic Identifying Wafer Defect Patterns with a 1D Convolutional Neural Network. Using the extensive WM-811K dataset, which is based on actual semiconductor manufacturing operations, the suggested framework can overcome the major issues associated with the imbalance of data, the difference in the size of wafer maps, and the low-contrast defects. A comprehensive preparation workflow that includes data cleansing, mapping pixel intensities, RGB conversion, resizing of images, and data augmentation had an immensely important positive impact on the strength of the model and the quality of the data. Experimental findings indicate that 1D-CNN model has high classification performance, as its accuracy and AUC-ROC are 99.0 and 99.0, respectively, and both the F1-score, recall, and accuracy scores are all balanced. The analysis of learning curves and confusion matrix also ensures that convergence is stable, there is great generalization, and minimal misclassification. The accuracy and dependability of the suggested model demonstrate its advantages over the current approaches. Together, the results confirm the usefulness of the 1D-CNN framework in the real-world defects inspection in the wafer,

which provides a scalable and precise method of quality control within the semiconductor production process.

The future progress of the research will aim at investigating the ideas of hybrid deep learning architectures, including the fusion of CNNs with attention mechanisms, to enhance the classification accuracy. Also, the framework can be extended to multi-class defect classification and real-time industrial application, which will increase the applicability of this framework in semiconductor manufacturing.

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